AMENDMENTS TO THE SPECIFICATION:

Page 4, amend paragraph [0008] as:

[0008] The conventional two-stage approach, thus has two main drawbacks: (1) [[lager]] larger circuitry due to the use of frequency and block de-interleaving buffer and (2) higher power consumption due to higher processing rate for de-interleaving the interleaved data.

Page 9, delete paragraph [0023].

Page 9, before paragraph [0024], add the following new paragraph:

Consequently, the memory location for writing data after demodulation into the de-interleaving memory 303 is calculated as

$$Write\_address = segment\_pointer\_wr + group\_pointer\_wr + sub\text{-}group\_pointer\_wr + cell\_pointer\_wr. \quad (1)$$

In the following, how to calculate each pointer is further described.

Page 11, delete paragraph [0028].

Page 11, before paragraph [0029], add the following new paragraph:

Finally, the write address is determined by summing up the four pointers, *segment_pointer_wr*, *group_pointer_wr*, *sub-group_pointer_wr* and *cell_pointer_wr*. The write address can be rewritten in a more specific way as follows.

$$Write\_address = ofdm\_symbol\_no * segment\_size + Q(deitlvfreq\_no/16) * group\_size$$

$$+ LUT(deitlyfreq\_no(mod\ 16)) + cell\_pointer\_wr \quad (5)$$

Page 13, amend paragraph [0034] as:

[0034] Referring back to the equations for *Write_address* and *Read_address*, it can be seen that the computation for either *Write_address* or *Read_address* needs two multiplications, a division of performing quotient and modulus operations, a look up table, and a cyclic counting as well as a summation which sums up the resultant values from the two multiplications, the look up table, and the counting. In other words, the address generator in the embodiment of FIG. 5 may include ~~includes~~ two multipliers 511 and 512, a divider 503, a quotient unit 504, a remainder unit 505, a look up table 506, a counter 507, and an adder 508. Note that in DAB system, the divider with divisor 16 can be easily implemented using shift registers since the divisor 16 is an integer power of two. Therefore, implementation of the address generator is relatively simple.

Pages 13-14, amend paragraph [0035] as:

[0035] It is also notable that there is no [[any]] additional buffering between the demodulator and the de-interleaving memory 303 according to the present invention. By using the de-interleaving memory 303 combined with memory address computation for the interleaved data, frequency de-interleaving, block de-interleaving, and time de-interleaving are performed in one-stage approach in the COFDM receiver. All digital I, Q components of the plurality of phase-modulated sub-carriers ~~sub-carries~~ in the received DAB signal can be saved in the same memory, i.e. the de-interleaving memory 303 of the invention.